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QUESTION BANK (DESCRIPTIVE)

Subject with Code : DIGITAL ELECTRONICS(18EC0444) **Course & Branch**: B.Tech - EEE

Year & Sem: II-B.Tech & II-Sem **Regulation:** R18

UNIT –I

BINARY SYSTEMS

1. Convert the given decimal number 234 to binary, octal, hexadecimal and BCD equivalent. **(10M)L1, CO.1**
2. Perform the following
   a) Subtraction by using 1's complement for the given 10101 - 11011. **(5M)L3, CO.1**
   b) Subtraction by using 2's complement for the given 111001-1010. **(5M)L3, CO.1**
3. A) Convert the following to Decimal and then to Octal. (i) $(4234)_{16}$ (ii) $(10010011)_2$. **(5M)L1, CO.1**
   b) Convert the following to Decimal and then to Hexadecimal. (i) 12348 (ii) 110011112 **(5M)L1, CO.1**
4. Simplify the following Boolean expression:
   (a) F = (A+B)(A'+C)(B+C). **(5M)L3, CO.1**
   (b) F = XY+XYZ+XYZ'+X'YZ **(5M)L3, CO.1**
5. A) Explain Different Types of binary codes and give the examples **(5M)L3, CO.1**
   b) Simplify the following Boolean functions to minimum number of literals **(5M)L3, CO.1**
   (i) xyz + x'y + xyz'. (ii) xz + x'yz.
6. Convert the following to Decimal and then to Octal **(10M)L1, CO.1**
   (A) 1234_{16} (b) $12EF_{16}$ (c) 10110011_2 (d) 10001111_2 (e) 352_{10}
   (f) 999_{10}
7. Express the function Y=A+B'C in (i)Canonical SOP form (ii) Canonical POS form **(10M)L3, CO.1**

8. (A)What is Switching Functions? Explain switching functions. **(5M)L1, CO.1**
(B) Simplify the following Boolean functions to minimum number of literals: **(5M)L3, CO.1**
F = ABC + ABC' + A'B

9. Explain about canonical SOP and POS forms. **(10M)** L3,CO.2

10. Convert the following to binary and then to gray code. **(10M)L1, CO.1**
(A) $(1AD5)_{16}$ (b) $(BC54)_{16}$ (c) $(237)_8$ (d) $(164)_{10}$ (e) $(323)_8$

UNIT –II

GATE–LEVELMINIMIZATION AND COMBINATIONALLOGIC

1. A) Minimize the following Boolean function using K-Map **(5M)L2, CO.1**
   F(A, B, C, D)= Σm(0, 2, 4, 6, 8, 10, 12, 14).
   B) What is Decoder ?design3:8 decoder **(5M)L2, CO.1**
2. Minimize the given Boolean function F(A,B,C,D) = Σ m(0,1,2,3,6,7,13,15) using tabulation method and implement using basic gates **(10M)L2, CO.1**
3. Simplify the following Boolean expressions using K-map **(10M)L3, CO.1**
   F(W,X,Y,Z)= XZ+W'XY'+WXY+W'YZ+WY'Z
4. Design 2 bit comparator with Logic diagram. **(5M)L3, CO.1**
5. A) Simplify the following expression using the K-map for the 3-variable. **(5M)L3, CO.1**
   Y = AB'C+A'BC+A'B'C+A'B'C'+AB'C'
   B) Simplify the Boolean function F(A,B,C,D)=∑m(1,3,7,11,15)+d(0,2,5) **(5M)L3, CO.1**
6. Minimize the given Boolean function F(A,B,C,D) = Σ m(0,2,3,6,7,8,10,12,13) using tabulation method and implement using basic gates **(10M)L2, CO.1**
7 Design 32:1 Mux using two 16:1 Muxs and one 2:1 Mux. **(10M) L5 CO.2**
8. Design & implement Half Adder and Full Adder with truth table. **(10M)L1, L3 CO.2**
9. A)Implement the fallowing Boolean function with 8:1 multiplexer.
   F(A,B,C,D)=∑m(0,2,6,10,12,13)+d(3,8,14) **(5M)L2, CO.2**
   B)Implement the fallowing Boolean function with 8:1 multiplexer.
   F(A,B,C,D)=πM(0,3,5,6,8,9,10,12,14) **(5M)L2, CO.2**
10. What is Demultiplexer? Desingn1:8 Demultiplexer using 1:4 Demultiplexers. **(10M)L3, CO.2**

UNIT –III

SEQUENTIAL LOGIC DESIGN

1. A) Design D Flip Flop by using SR Flip Flop Explain the operation with truth table. **(6M)L1, CO.3**

   b) Write the differences between combinational and sequential circuits. **(4M)L5, CO.2**

2. A) Explain working of Master Slave Flip flop with neat diagram. **(5M)L3, CO.2**

   b) Design T Flip Flop by using JK Flip Flop and draw the timing diagram. **(5M)L1, CO.2**

3. Draw the circuit of JK flip flop using NAND gates and explain its operation. **(10M)L3, CO.3**

4. A) Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram. **(5M)L1, CO.3**

   b) Convert D flip flop into JK-flip flop. Draw and explain the logic diagram. **(5M)L3, CO.2**

5. What is Register Explain i) Parallel in Parallel out Register **(10M)L3, CO.3**
   ii) Series in Parallel out Register

6. Design and implement 3-bit ripple counter using J-K flip flop. Draw the state diagram, logic diagram and timing diagram for the same. **(10M)L1,L3, CO.3**

7. With a neat sketch explain MOD 6 Johnson counter using D FF. **IES 2015** **(10M)L3, CO.2**

8. Implement 6-bit ring counter using suitable shift register. Briefly describe its operation. **(10M)L3, CO.2**

9. Design D Flip Flop by using SR Flip Flop Explain the operation with truth table. **(10M)L3, CO.3**

10. Design MOD-10 Asynchronous counter by using T-Flip flop **(10M)L3, CO.3**

UNIT-IV
LOGIC FAMILIES

1. Perform the analysis of standard TTL NAND gate and give its characteristics. **[10M][L4][CO3]**
2. Give the classification of integrated circuits and compare the various logic families. **[10M][L2][CO2]**
3. What is meant by Tristate logic? Draw the circuit of Tristate TTL logic and explain the functions. **[10M][L4][CO4]**
4. Explain the following specifications **[10M][L2][CO2]**
   (i) Fan out
   (ii)Fan out
5. What is meant by ECL? Draw the circuit of Tristate ECL logic and explain the functions. **[10M][L2][CO2]**
6. Explain about TTL to CMOS interfacing **[10M][L4][CO2]**
7. Compare TTL, ECL and CMOS **[10M][L1][CO2]**
8. Explain the following specifications **[10M][L2][CO2]**
   (i) Propagation delay.
   (ii)Noise margin.
9. Explaine about CMOS families. **[10M][L2][CO2]**
10. Explain about Logic gates. with symbols and truth tables. **[10M][L2][CO2]**

UNIT –V
SEMICONDUCTOR MEMORIES AND PROGRAMMABLE LOGIC DEVICES

1. Implement the following Boolean function using PLA **(10M)L3, CO.4**
   (i)F(w,x,y,z) = Σm(0,1,3,5,9,13) (ii)F(w,x,y,z)) = Σm(0,2,4,5,7,9,11,15)
2. Implement the following Boolean function using PAL. **(10M)L3, CO.4**
   (i)A(w,x,y,z) = Σm(0,2,6,7,8,9,12,13) (ii)B(w,x,y,z)) = Σm(0,2,6,7,8,9,12,13,14)
   (iii)C(w,x,y,z) = Σm(1,3,4,6,10,12,13) (iv)D(w,x,y,z)) = Σm(1,3,4,6,9,12,14)
3. Explain About Content Addressable Memory (CAM) charge de coupled devicememory (CCD) **(10M)L3, CO.4**
4. Implement PLA circuit for the following functions F1(A,B,C)= Σm(3,5,6,7), F2(A,B,C)= Σm(0,2,4,7). **(10M)L3, CO.4**
5. Differentiate among ROM, PROM ,DROM ,EPROM, EEPROM, RAM. (5M)L3, CO.3 **(10M)L1, CO.4**
6. Explain the minimization procedure for determining the set of equivalent state of a specified machine M. **(10M)L2, CO.4**
7. A) What is ROM organization? Explain about Different types of ROM. **(10M)L3, CO.4**
8. Compare three combinational circuits: PLA, PAL and PROM **(10M)L3, CO.3**
9. Give the logic implementation of a 32x4 bit ROM using a decoder of a suitable figure. **(10M)L3, CO.4**
10. What is RAM organization? Explain about Different types of RAM. **(10M)L3, CO.4**

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